# Datasheet

## DCU040
**Version 1.1**

## Revision History

| Revision | Date | Change Description |
|----------|------|-------------------|
| 1.0 | Apr-2021 | Preliminary version |
| 1.1 | Jul-2023 | Updated pin-16 description & Module picture |
| | | |
| | | |

# Table of Contents

# 1. Introduction

The DCU040 is fully interoperable with IEEE® 802.15.4 HRP UWB standard. It is designed to operate worldwide with support of 500MHz UWB channels 5 (6489.6MHz) to 9 (7987.2MHz). It enables high-precision positioning applications with a non-Line-of-Sight precision of 5±10cm. It is a (SMD) Surface Mount Device designed to be easily mounted over custom Printed Circuit Boards (PCB) to deploy.
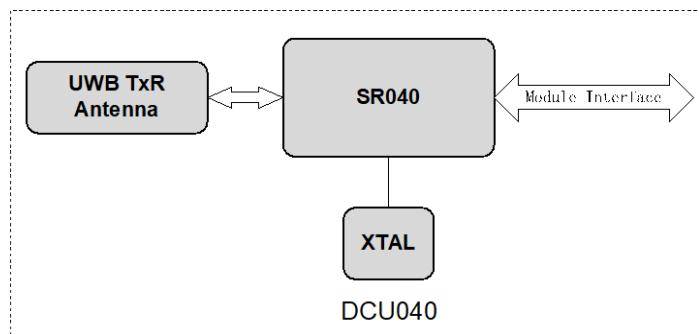
## 1.1. Key Features



| Name | DCU040 |
|---|---|
| Antenna Type | PCB patch |
| Size | Size 15.7 x 16.75 x 2mm |
| Communication Interface | SPI |
| Main Chip | SR040 |
| Channel | 5, 9 |
| Frequency range | 6.24GHz~8.24GHz |
| Supply Voltage | 1.8 ~ 3.6V |
| Max Output Power (EIRP) | 14.7 dBm |

## 1.2. Applications

The perfect TAG for High Precision RTLS & Industrial application. Ideally suited as TAG&TRACKER for IoT Consumer & Smart Home application.

## 1.3. Block Diagram



## 2. Electrical characteristics

## 2.1. Recommended operating conditions

When the input voltage of the module is lower than the rated operating voltage, the operation will be unstable. Input voltage higher than the maximum rating will cause permanent damage to the module. At the same time, working under the maximum rating for a long time also affects the stability of the module.

| Parameter | Min | Type | Max | Unit | Conditions/Notes |
|---|---|---|---|---|---|
| Operating Temperature | −30 | | +85 | ˚C | |
| Supply Voltage (Vdd) | 2.4 | 3.3 | 3.6 | V | All specification parameters fulfilled |
| | 1.8 | | 2.4 | V | • Device fully functional<br>• TX PA peak power shall not be set higher than +9dBm |
| HIGH level input voltage ($V_{IH}$) | 1.26 | | Vdd+0.5 | V | |
| LOW level input voltage ($V_{IL}$) | −0.6 | – | 0.54 | V | |
| HIGH level output voltage ($V_{OH}$) | Vdd−0.5 | – | Vdd | V | |
| LOW level output voltage ($V_{OL}$) | – | – | 0.2 | V | |

## 2.2. RF characteristics

| Parameter | | Min | Type | Max | Unit | Conditions/Notes |
|---|---|---|---|---|---|---|
| Frequency range | | 6240 | | 8240 | MHz | Channel 5 and 9 |
| Channel bandwidth | | | 500 | | MHz | |
| Power level range | | | 32 | | dB | |
| Power level step | | | 0.25 | | dB | |
| Rx Sensitivity (±10ppm carrier Offset) | Channel 5 | | | -92 | dBm | 64 preamble, 6.8Mbps data rate |
| | Channel 9 | | | -92 | dBm | 64 preamble, 6.8Mbps data rate |

## 2.3. Antenna specifications

| Antenna Type | PCB Embedded |
|---|---|
| Antenna Polarization | Linear |
| Peak directivity | 4.5dBi @CH5 |
| | 3.8dBi @CH9 |
| Radiation efficiency | 60% @ CH5 |
| | 77% @ CH9 |
| Frequency range | 6.0 ~ 8.5GHz |
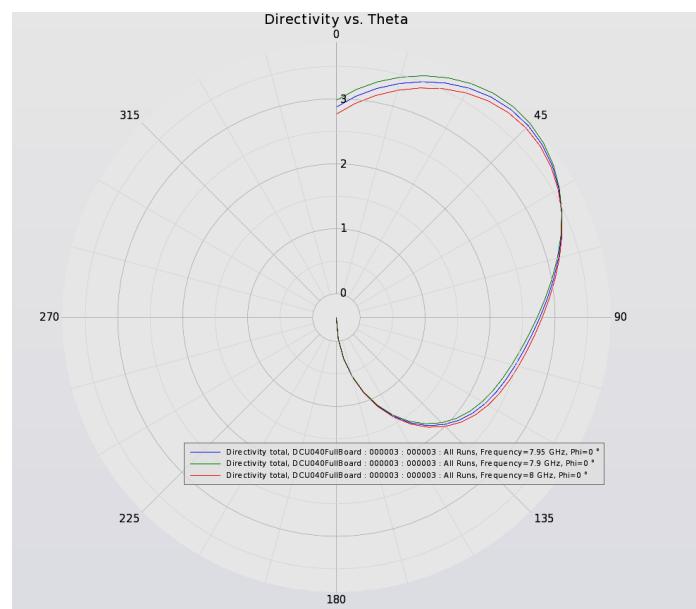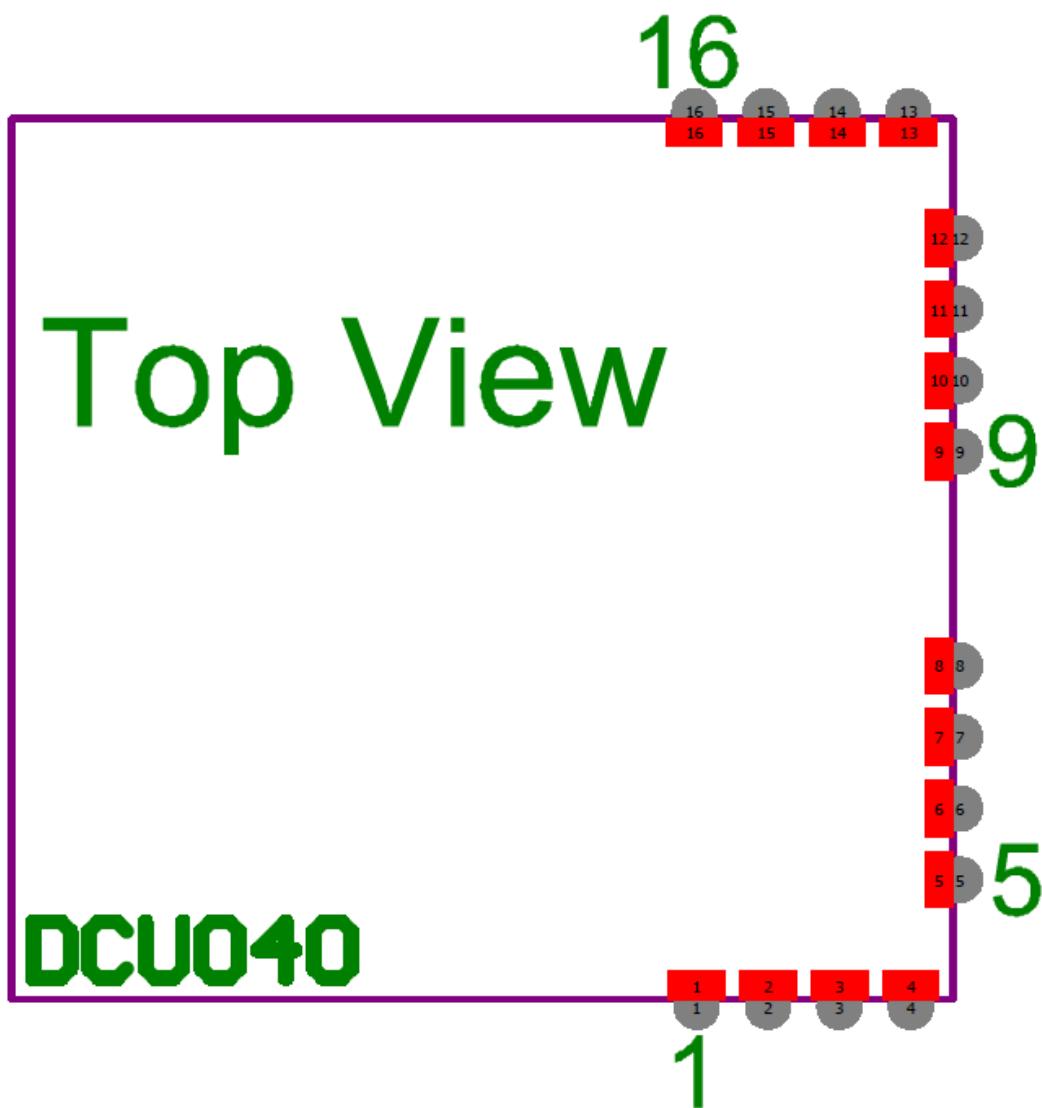


*Fig. 1 Directivity at channel 9 center frequency and ch9 center frequency ±500MHz*

# 3. Module Package
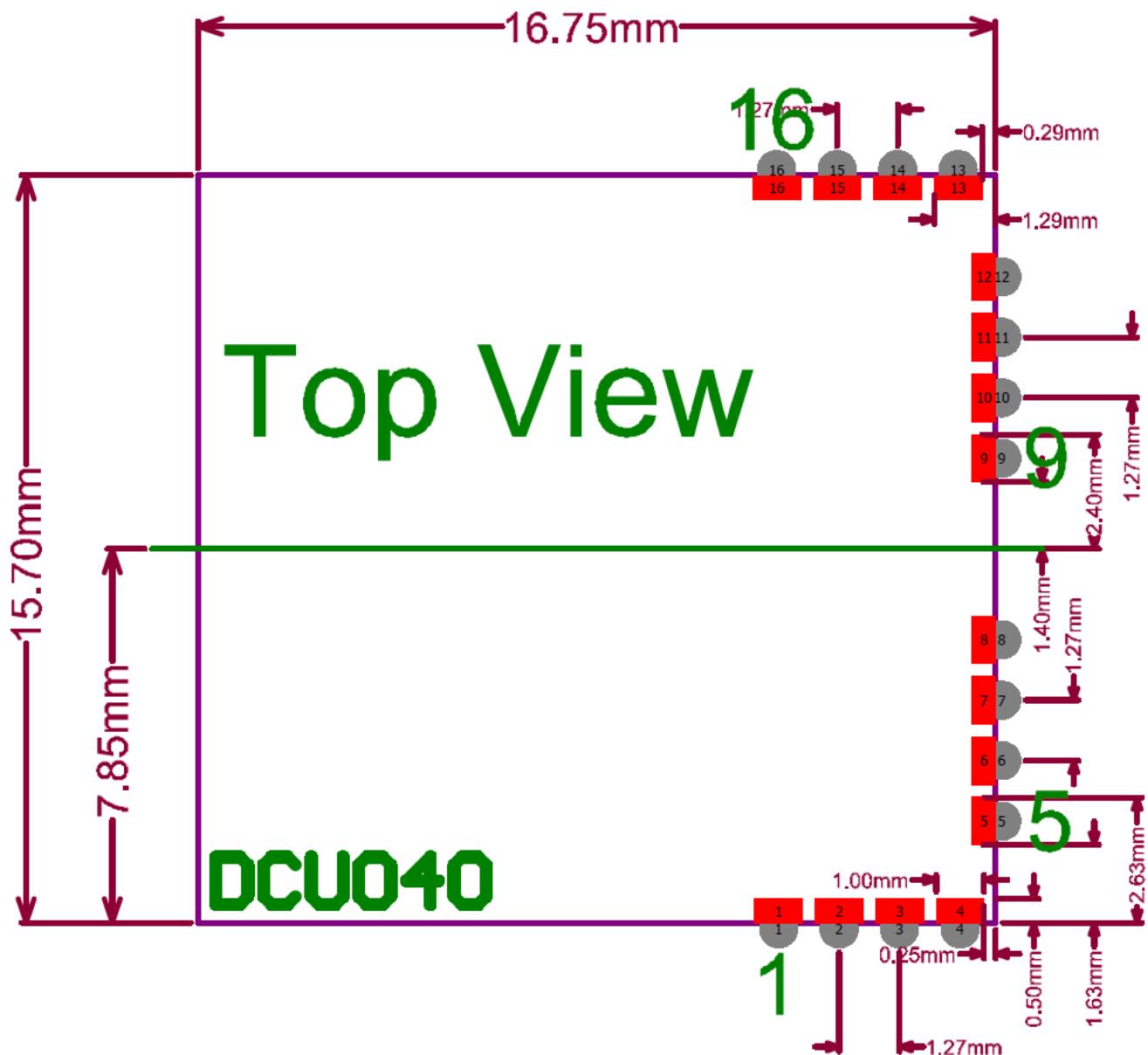
## 3.1. Pinout Description
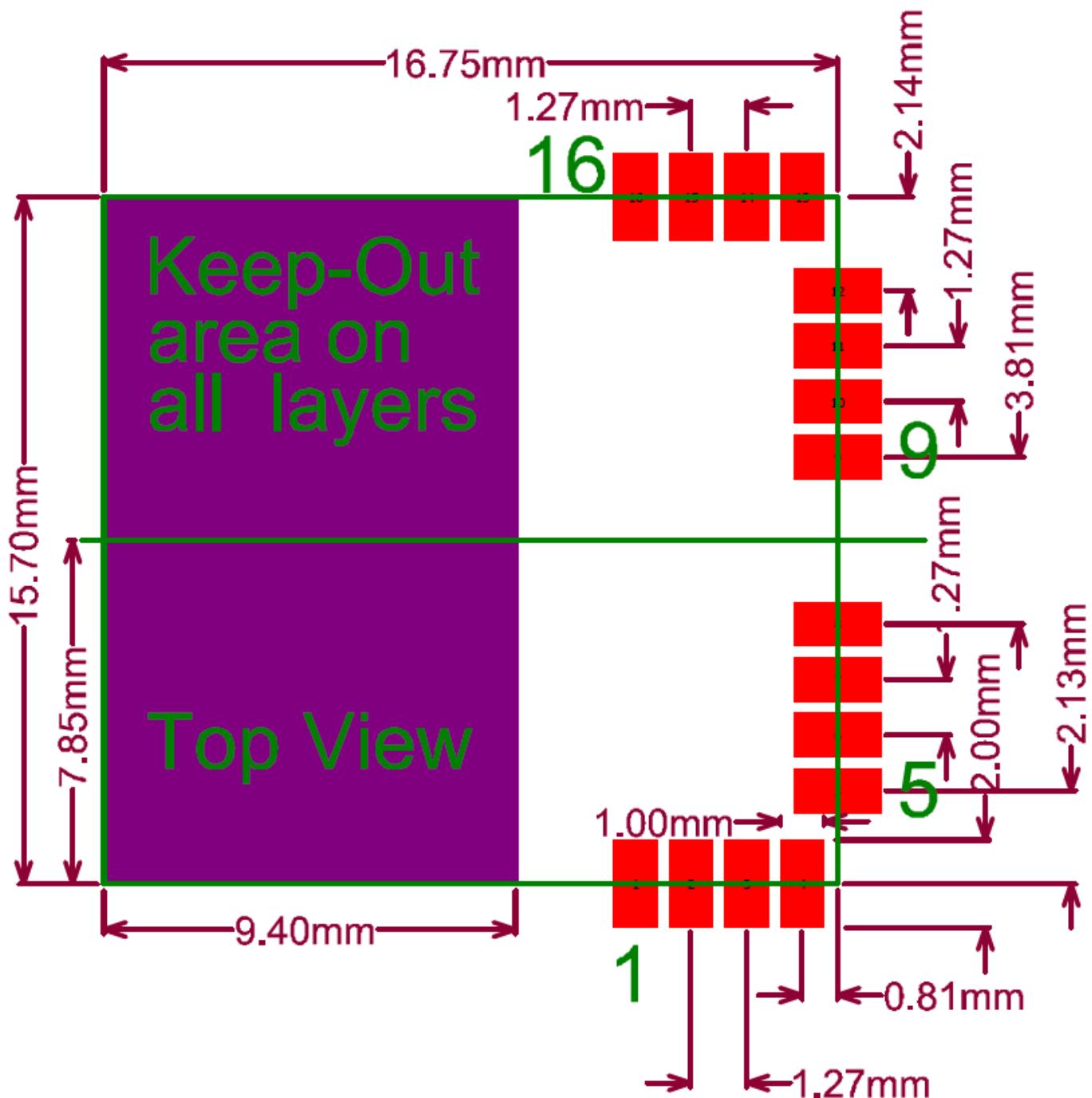
## 3.2. Pin Description Box

| Pin | Pin Name | Pin Type | Description |
|-----|----------|----------|-------------|
| 1 | P12/TX | O | GPIO TX - Data output in UART operation |
| 2 | SWCLK | I/O | Serial Wire Debug (SWD) clock, internal pull-up resistor |
| 3 | SWDIO | I/O | Serial Wire Debug (SWD) data, internal pull-up resistor |
| 4 | P13 | I/O | GPIO CS2_N - Second Chip Select (active low) output in SPI Master operation<br>RTS - "Request To Send" in UART operation |
| 5 | P14/CS_N | I/O | GPIO CS_N - Chip Select (active low); output in SPI Master operation; input in<br>SPI Slave operation |
| 6 | P21/SDI | I | GPIO SDI - Data input for SPI full duplex operation |
| 7 | P17/SCLK | I/O | GPIO SCLK - Data clock for SPI operation; output in SPI Master operation; input<br>in SPI Slave operation |
| 8 | P20/SDIO | I/O | GPIO SDIO - Data I/O for SPI operation; output in full duplex operation; input/<br>output in half-duplex operation |
| 9 | GND | G | Ground |
| 10 | P15/INT_N | O | GPIO INT_N - Interrupt output (active low) in 6-wire SPI operation |
| 11 | P16/RDY_N | O | GPIO RDY_N - Ready output (active low) in 6-wire SPI operation |
| 12 | RST_N | I | Reset input (active low), internal pull-up resistor |
| 13 | P11/RX | I | GPIO RX - Data input in UART operation |
| 14 | P10 | I/O | GPIO CTS - "Clear To Send" in UART operation PA_ENBL - Gating signal for an optional external PA |
| 15 | VBAT | P | Power supply for digital I/Os and power supply for the chip via current limiter |
| 16 | VLIM | P | Power supply for digital domain and XTAL |

## 3.3.Package outline
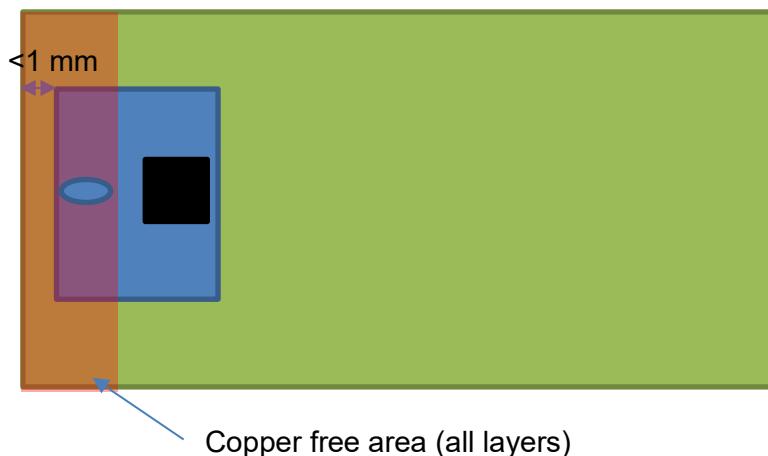
## 3.4. Recommended PCB Footprint

## 3.5 Host board mounting

DCU040 is designed to be mounted onto a host board. Suggested host-board thickness is 0.8mm and it should be greater than 0.5mm. The DCU040 is preferably mounted close to the host board edge, as shown next. Maximum distance to the edge should be up to 1mm.



Copper free area (all layers)
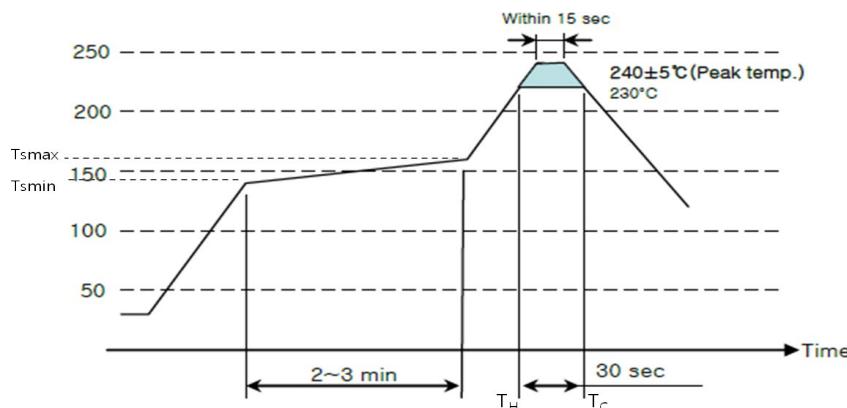
# 4. Soldering Condition

## 4.1. Manual Soldering – Pb Free

Soldering Temperature: 360ºC ± 5ºC, 5sec max.
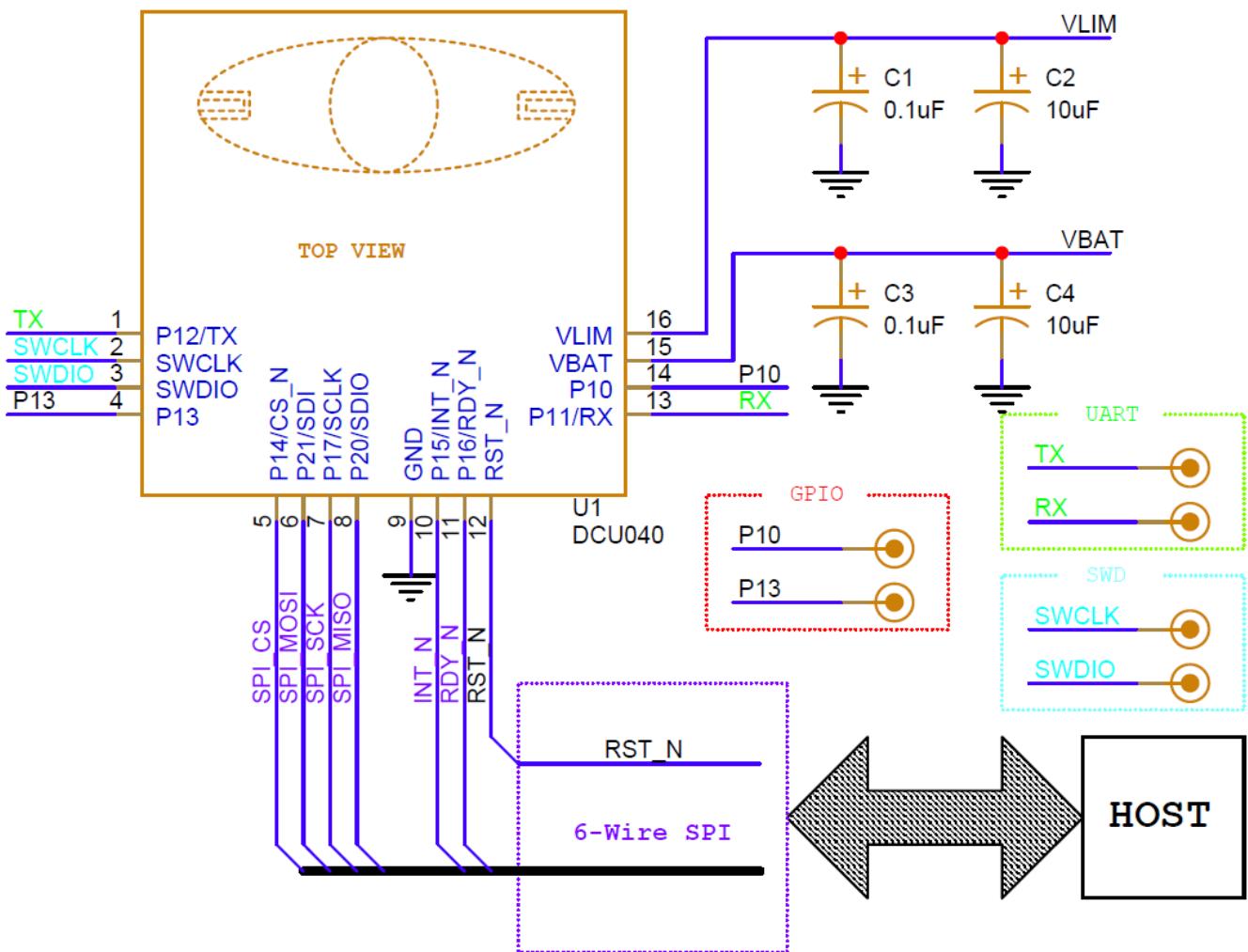
## 4.2. Recommended Reflow Condition – Pb Free



| Profile Feature | Pb-Free Assembly |
|---|---|
| Preheat | |
| -Temperature Min (Tsmin) | 140˚C |
| -Temperature Typical (Tstypical) | 150˚C |
| -Temperature Max (Tsmax) | 160˚C |
| -Time Tsmin to Tsmax | 2 ~ 3 min |
| Peak Temperature | 240±5˚C |
| Time of actual peak temperature | Max. 15 seconds |
| Heating to Cool | |
| -Temperature Heating (TH) | 230˚C |
| -Temperature Cool (TC) | 230˚C |
| -Time TH to TC | 30 seconds |

# 5. Application design-in information

## 5.1 Reference schematics for DCU040



The key component values for the schematic are shown in

| Part code | Description | Value | Notes |
|-----------|-------------|-------|-------|
| C1,C3 | Multilayer Ceramic Capacitor, 0402, X7R | 100nF ±10% / 16V | |
| C2,C4 | Multilayer Ceramic Capacitor, 0402, X5R | 10µF ±10% / 16V | |

# 6. Regulatory approval

Regulatory approvals are pending.