Datasheet

TSR040

Version 1.0

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Revision History

Revision	Date	Change Description
1.0	Dec-2025	Preliminary version

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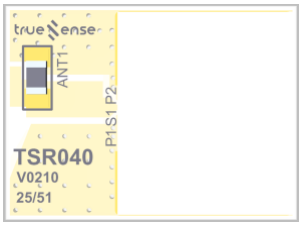
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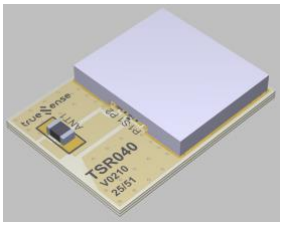
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1. Introduction

The TSR040 is fully interoperable with IEEE® 802.15.4 HRP UWB standard. It is designed to operate worldwide with support of 500MHz UWB channels 5 (6489.6MHz) to 9 (7987.2MHz). It enables high-precision positioning applications with a non-Line-of-Sight precision of 5±10cm. It is a (SMD) Surface Mount Device designed to be easily mounted over custom Printed Circuit Boards (PCB) to deploy.

1.1. Key Features





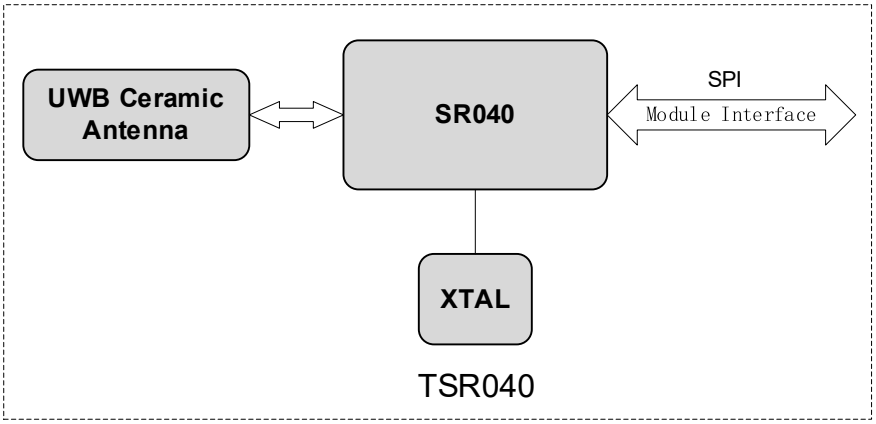
Name	TSR040
Antenna Type	Ceramic Antenna
Size	Size 13.0 x 17.8 x 2.5mm
Communication Interface	SPI
Main Chip	SR040
Channel	Ch 5 and CH 9
Frequency range	6.24GHz~8.24GHz
Supply Voltage	1.8 ~ 3.6V (Typ. 3.3V)
Max Output Power (EIRP)	+14.5 dBm

1.2. Applications

The perfect TAG for High Precision RTLS & Industrial application. Ideally suited as TAG & Tracker for IoT Consumer & Smart Home application.

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1.3. Block Diagram



2. Electrical characteristics

2.1. Recommended operating conditions

When the input voltage of the module is lower than the rated operating voltage, the operation will be unstable. Input voltage higher than the maximum rating will cause permanent damage to the module. At the same time, working under the maximum rating for a long time also affects the stability of the module.

Parameter	Min	Type	Max	Unit	Conditions/Notes
Operating Temperature	-30		+85	˚C	
Supply Voltage (Vdd)	2.4	3.3	3.6	V	All specification parameters fulfilled
	1.8		2.4	V	Device fully functional TX PA peak power shall not be set higher than +9dBm
HIGH level input voltage (V_{IH})	1.26		Vdd+0.5	V	
LOW level input voltage (V_{IL})	-0.6	-	0.54	V	
HIGH level output voltage (V_{OH})	Vdd-0.5	-	Vdd	V	
LOW level output voltage (V_{OL})	-	-	0.2	V	

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2.2. RF characteristics

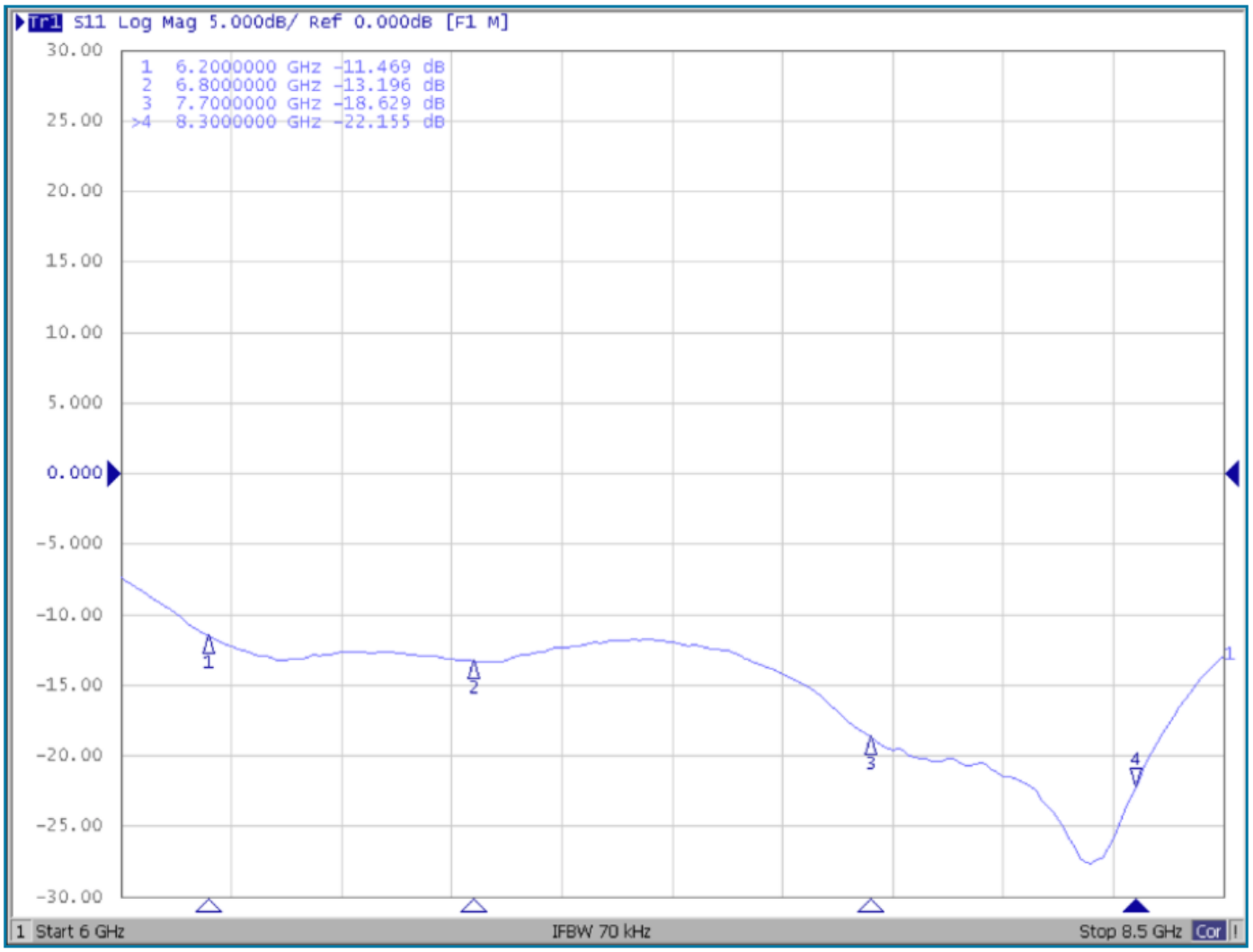
Parameter		Min	Type	Max	Unit	Conditions/Notes
Frequency range		6240		8240	MHz	Channel 5 and 9
Channel bandwidth			500		MHz	
Power level range			32		dB	
Power level step			0.25		dB	
Rx Sensitivity (±10ppm carrier Offset)	Channel 5			-92	dBm	64 preamble, 6.8Mbps data rate
	Channel 9			-92	dBm	64 preamble, 6.8Mbps data rate

2.3. Antenna specifications

Antenna Type	Ceramic Antenna
Antenna Polarization	Linear
Peak directivity	2.3dBi @CH5 2.5dBi @CH9
Radiation efficiency	52% @ CH5 62% @ CH9
Frequency range	6.2 ~ 8.3GHz

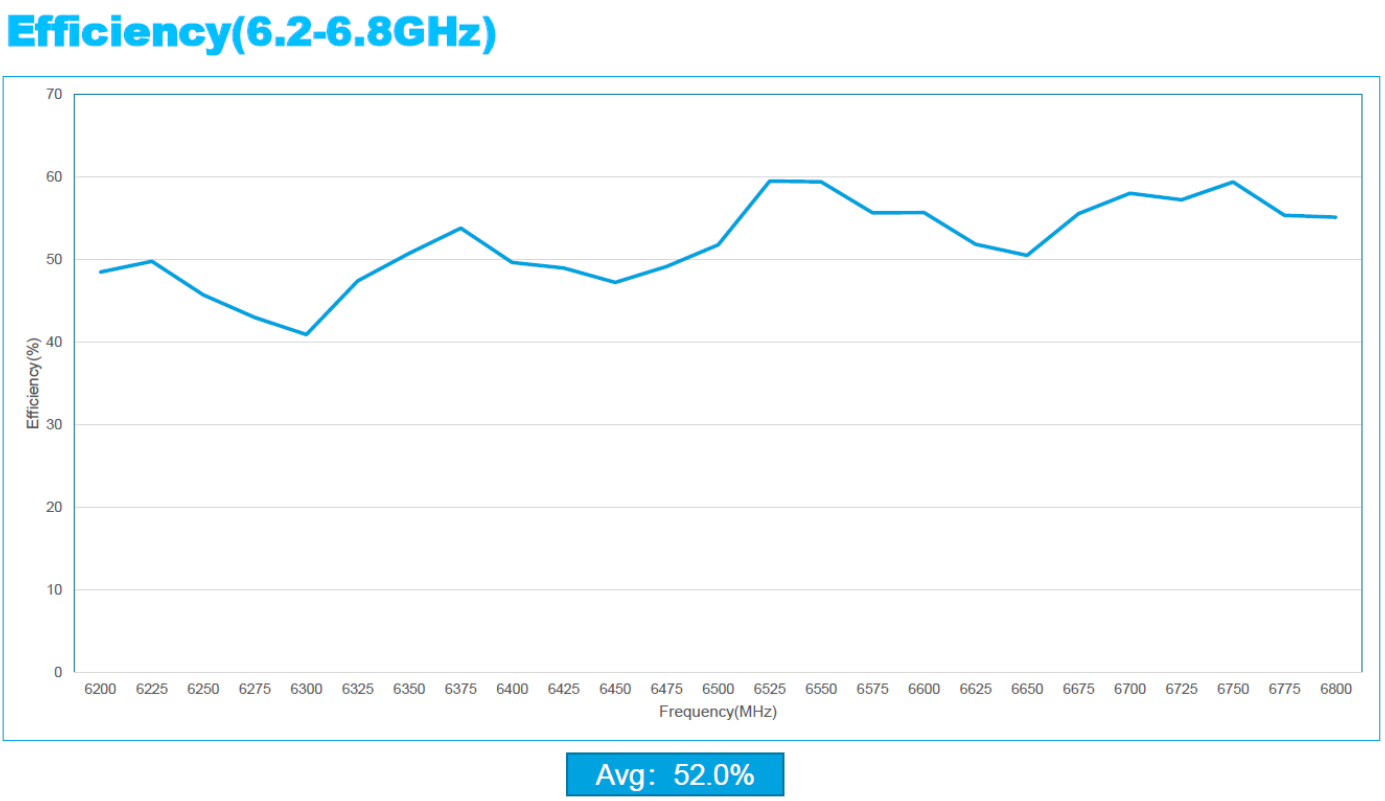
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2.3.1 Return Loss



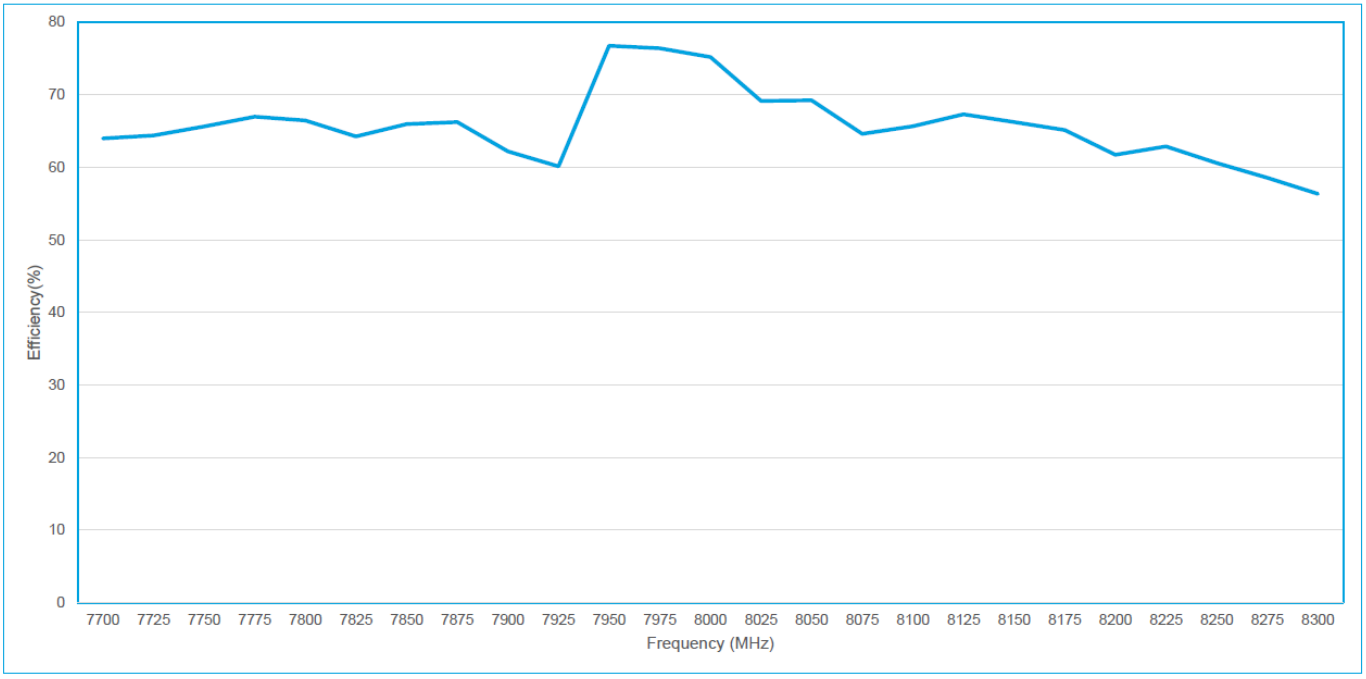
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2.3.2 Efficiency



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Efficiency(7.7-8.3GHz)

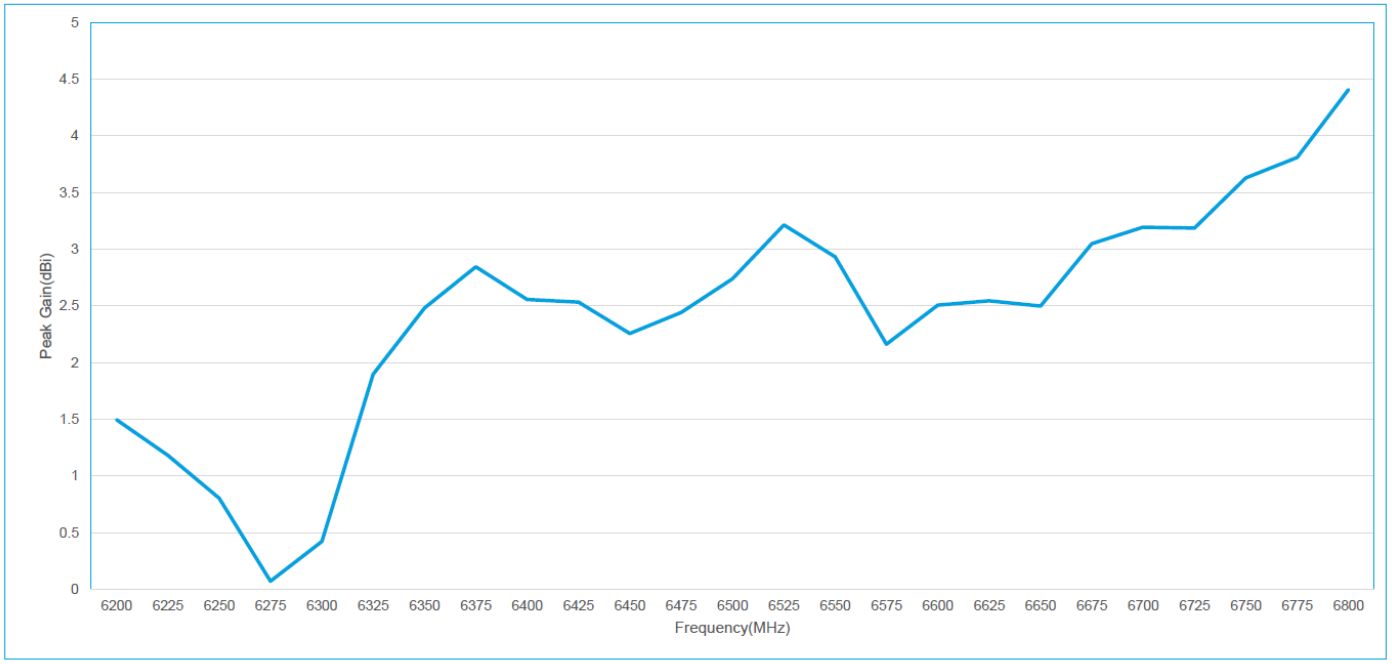


Avg: 62.1%

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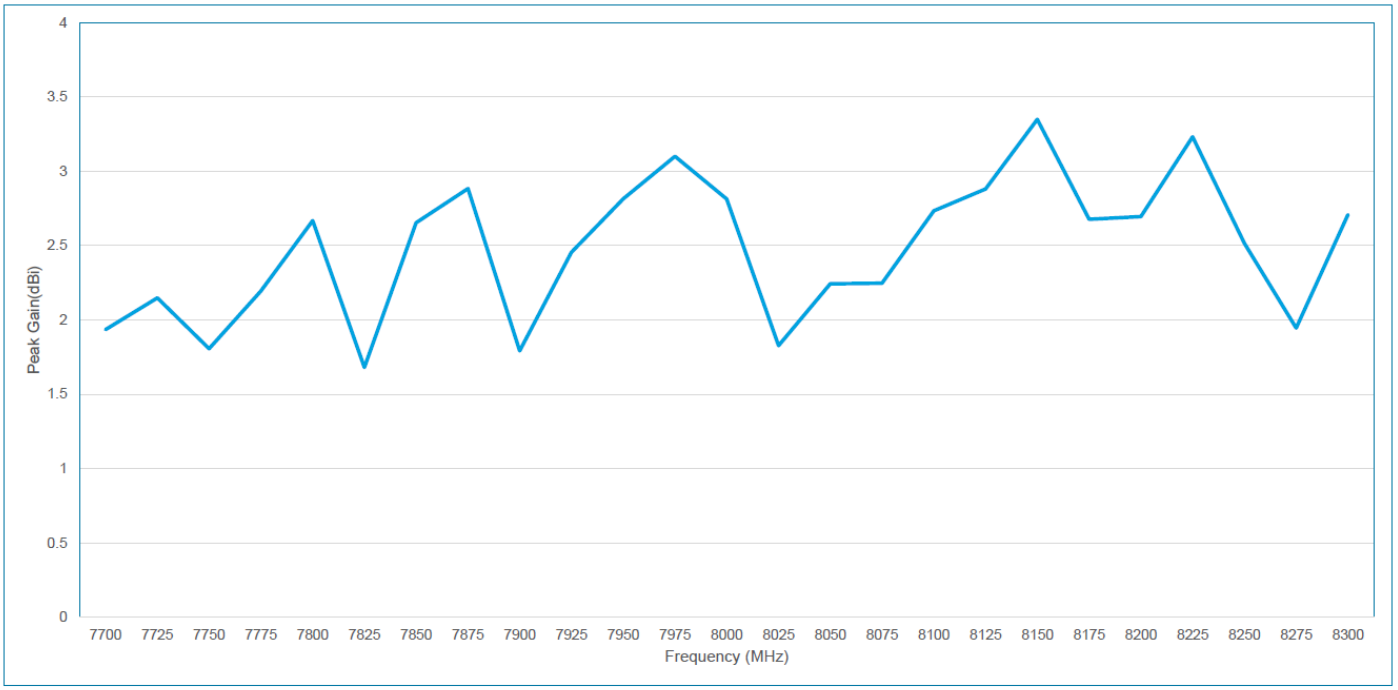
2.3.2 Peak Gain

Peak Gain(6.2-6.8GHz)



Avg: 2.3dBi

Peak Gain(7.7-8.3GHz)

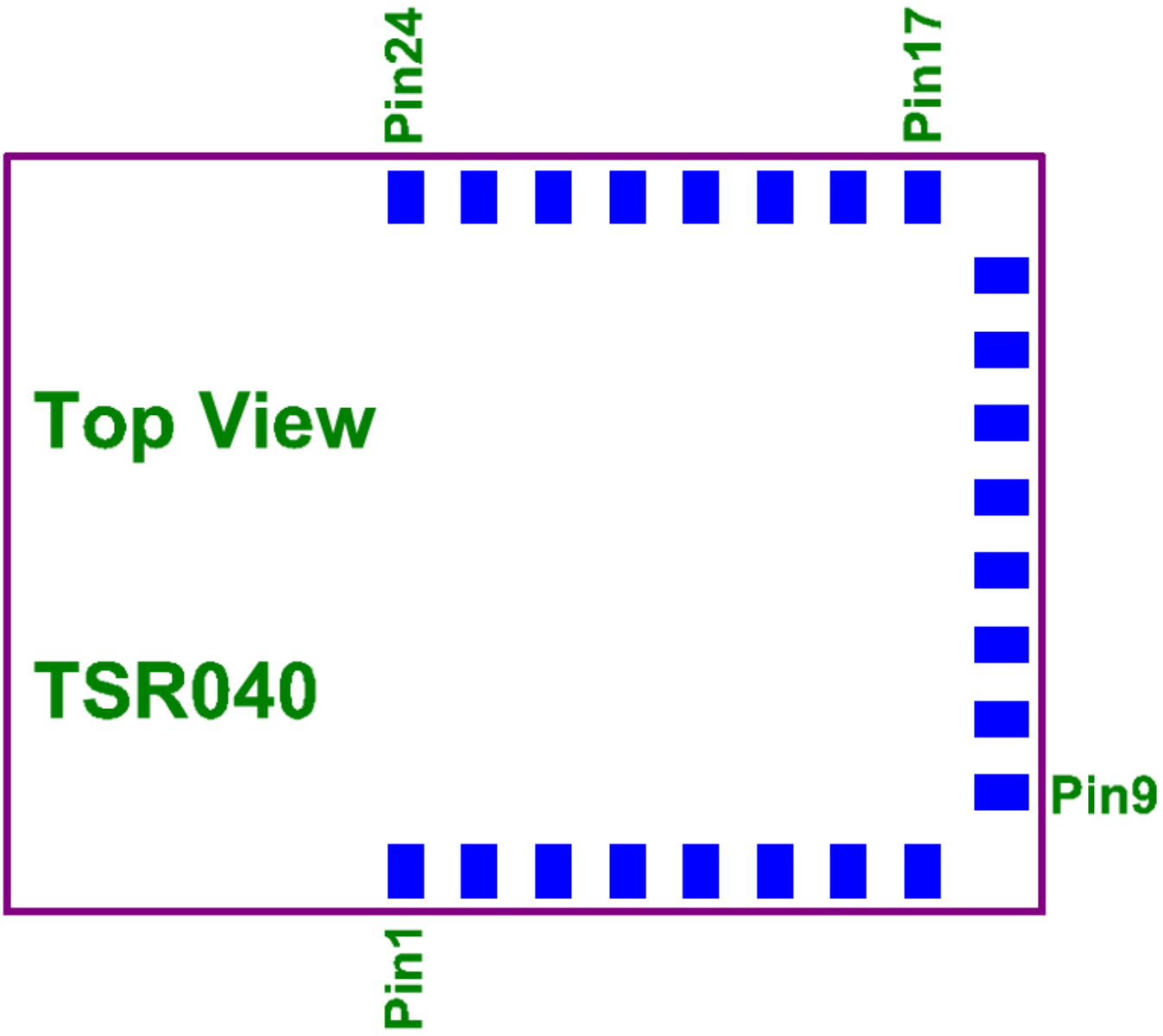


Avg: 2.5dBi

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3. Module Package

3.1. Pinout Description



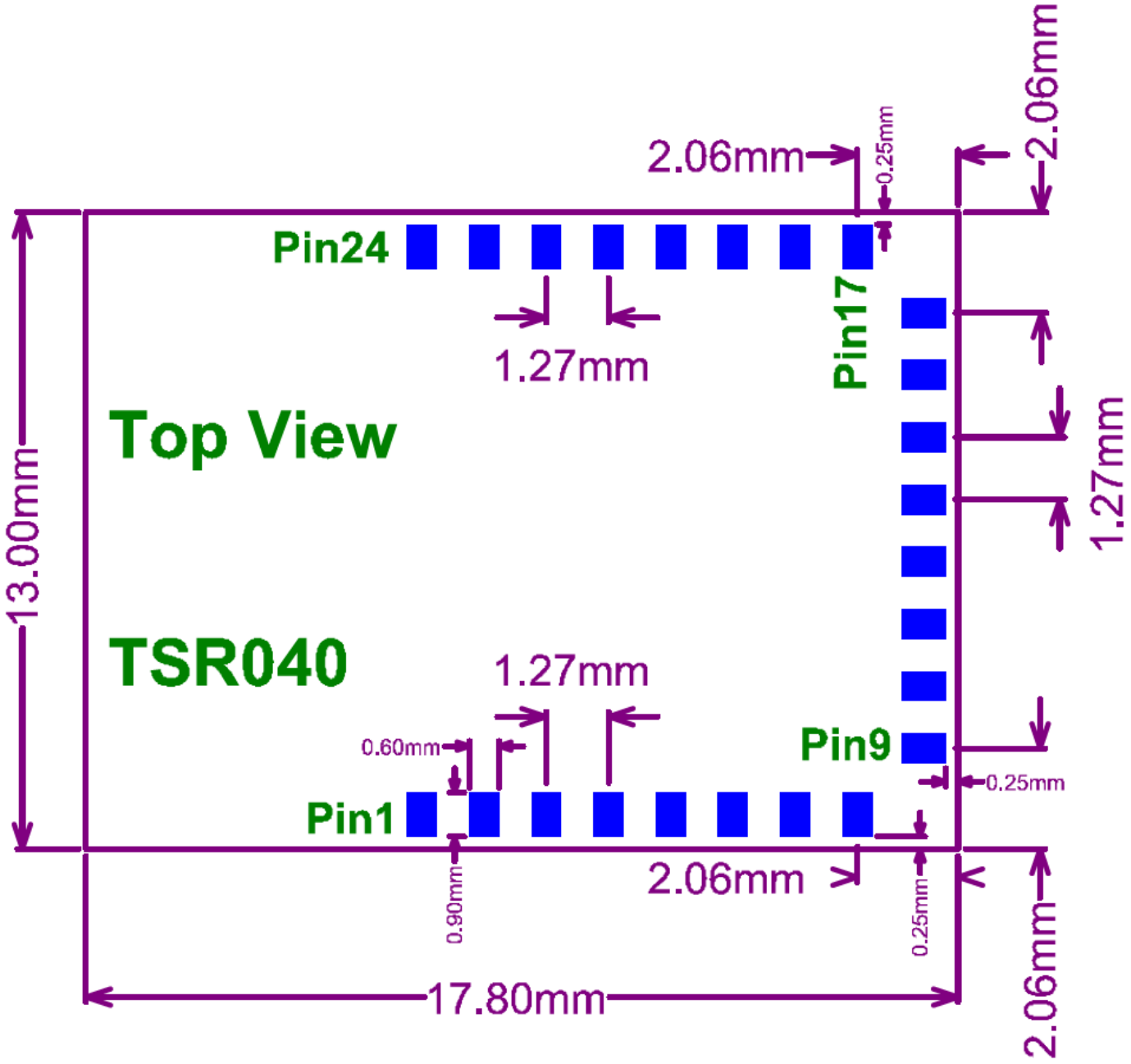
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3.2.Pin Description Box

Pin	Pin Name	Pin Type	Description
1	GND	G	Ground
2	P10	I/O	GPIO CTS - "Clear To Send" in UART operation PA_ENBL - Gating signal for an optional external PA
3	P11/RX	I	GPIO RX - Data input in UART operation
4	P12/TX	O	GPIO TX - Data output in UART operation
5	SWCLK	I/O	Serial Wire Debug (SWD) clock, internal pull-up resistor
6	SWDIO	I/O	Serial Wire Debug (SWD) data, internal pull-up resistor
7	P13	I/O	GPIO CS2_N - Second Chip Select (active low) output in SPI Master operation RTS - "Request To Send" in UART operation
8	GND	G	Ground
9	CS_N	I	Chip Select (active low), input in SPI Slave operation
10	MOSI	I	Data input when SPI is a slave in 4/6-wire operation, it clocks serial data in from this signal
11	SCLK	I	Data clock for SPI operation, input in SPI Slave operation
12	MISO	O	Data output when SPI is a slave in 4/6-wire operation
13	GND	G	Ground
14	INT_N	O	Interrupt output (active low) in 6-wire SPI operation
15	RDY_N	O	Ready output (active low) in 6-wire SPI operation
16	RST_N	I	Reset input (active low), internal pull-up resistor
17	GND	G	Ground
18	GND	G	Ground
19	VBAT	P	Power supply for digital I/Os and power supply for the chip via current limiter
20	VBAT	P	Power supply for digital I/Os and power supply for the chip via current limiter
21	VLIM	P	Power supply for digital domain and XTAL
22	VLIM	P	Power supply for digital domain and XTAL
23	GND	G	Ground
24	GND	G	Ground

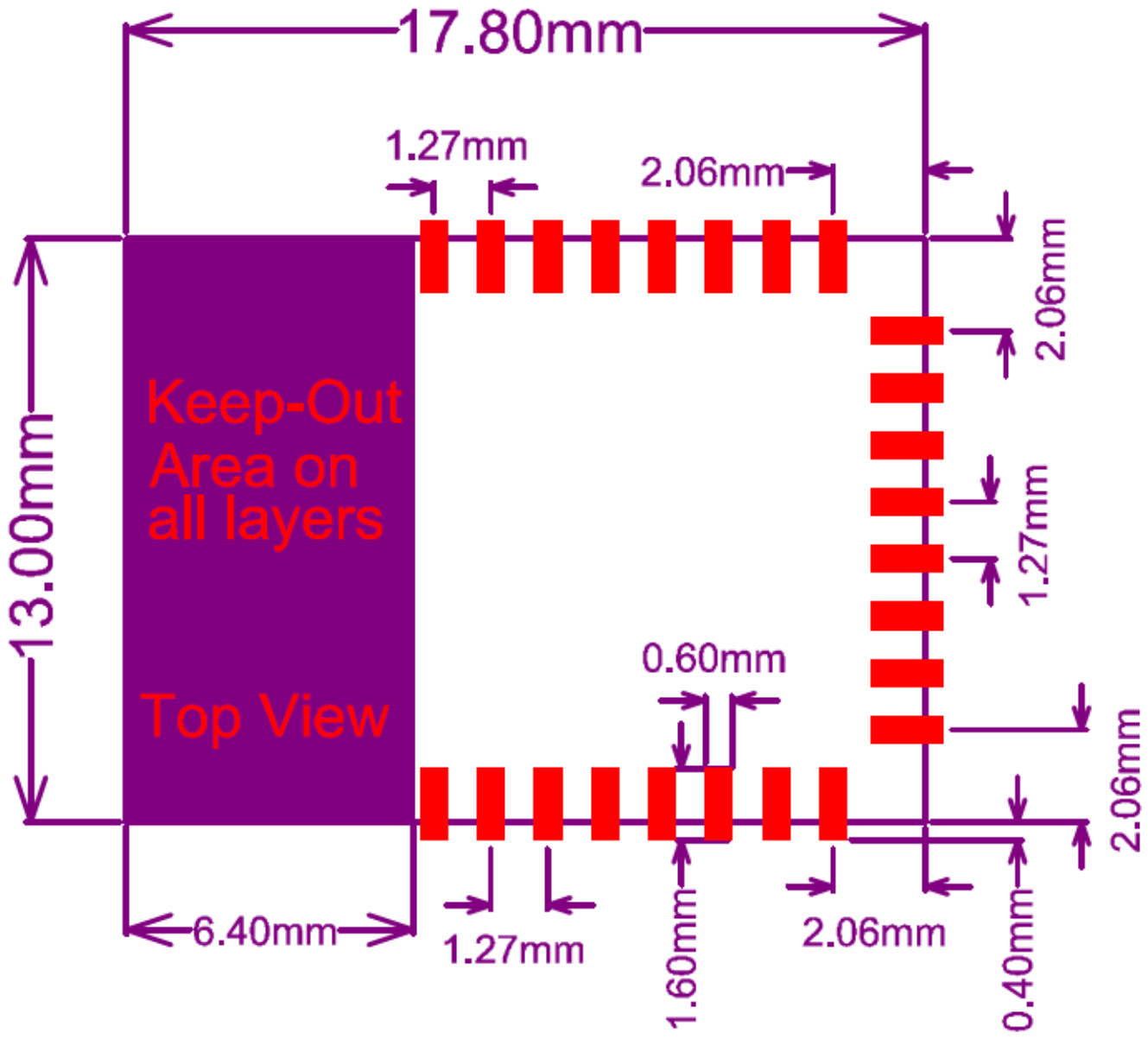
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3.3.Package outline



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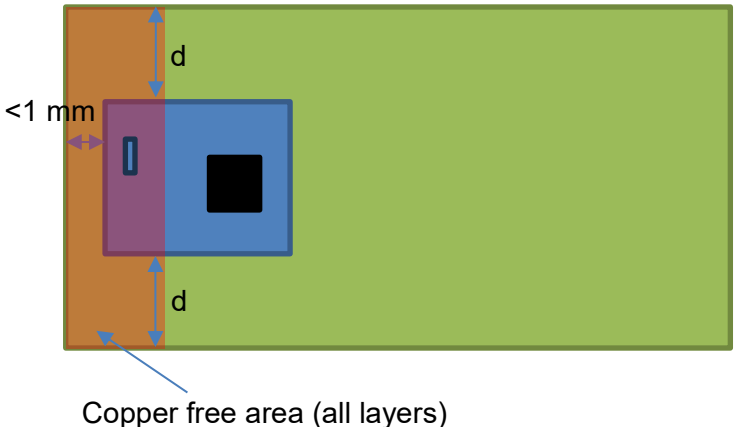
3.4. Recommended PCB Footprint



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3.5. Host board mounting

TSR040 is designed to be mounted onto a host board. The TSR040 is preferably mounted close to the host board edge, as shown next. Maximum distance to the edge should be up to 1mm.
It's also recommended to reserve a 10mm(d) spacing without metal(copper on PCB or components) at the left & right side of the module antenna area.



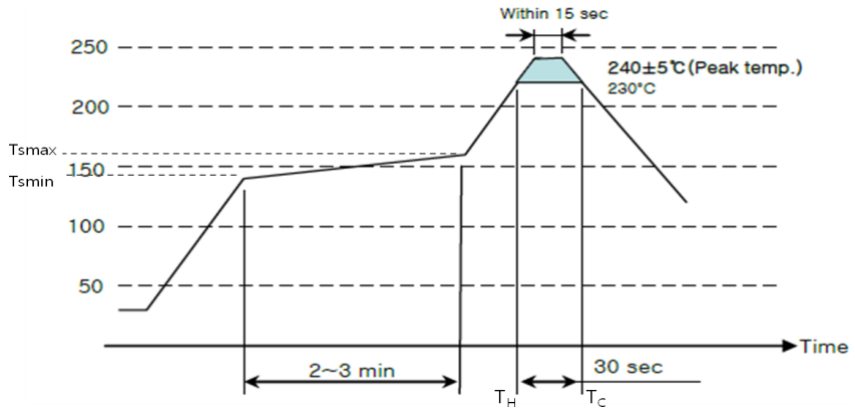
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4. Soldering Condition

4.1. Manual Soldering – Pb Free

Soldering Temperature: 360°C ± 5°C, 5sec max.

4.2. Recommended Reflow Condition – Pb Free

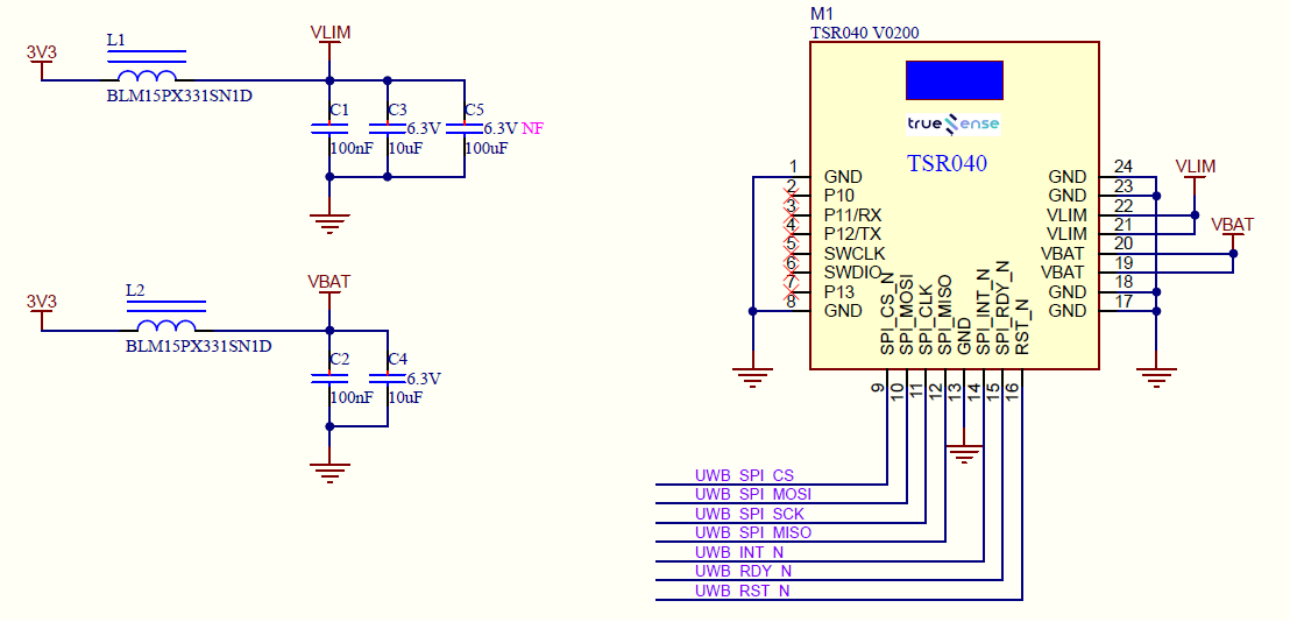


Profile Feature	Pb-Free Assembly
Preheat -Temperature Min (Tsmin) -Temperature Typical (Tstypical) -Temperature Max (Tsmax) -Time Tsmin to Tsmax	 140˚C 150˚C 160˚C 2 ~ 3 min
Peak Temperature	240±5˚C
Time of actual peak temperature	Max. 15 seconds
Heating to Cool -Temperature Heating (TH) -Temperature Cool (TC) -Time TH to TC	 230˚C 230˚C 30 seconds

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5. Application design-in information

5.1. Reference schematics for TSR040



*Note that:
(1) If TSR040 is powered by a coin battery (e.g. CR2032) which cannot deliver the high peak current demand of the module, a buffer capacitor must be connected to VLIM, which is C5 (typical value is 100uF), and must put L1 as NF(None-fitted);
(2) if TSR040 is powered by a regulator, typically a buffer capacitor is not required here. VLIM and VBAT can be connected to the same power source 3.3V. which is put C5 as NF, and L1 as fitted.

6. Regulatory approval

Regulatory approvals are pending.

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